REMARKS

For the reasons given below, Applicant requests reconsideration and withdrawal of all rejections.

35 U.S.C. §112 Rejection

Claim 1 was rejected as indefinite. Applicant respectfully disagrees. Although the Examiner's suggestion to cure the asserted indefiniteness appears innocuous, Applicant believes the amendment to be unnecessary, to effect no change of claim scope, to create (rather than remedy) indefiniteness, and to potentially give rise (as all amendments do) to unnecessary and unwarranted risk of prosecution history estoppel per the Festo decision. The language and grammar of claim 1 is clear and definite and there appears no reason to convert a clear, positive limitation written as an adjectival clause into a "wherein" clause. There is nothing magical about the word "wherein." Further, the Office Action does not explain how the claim is indefinite without "wherein." Applicant thus requests that the Examiner reconsider and, if the Examiner still believes the claim to be indefinite, that the Examiner explicate the indefiniteness. Accordingly, this rejection should now be withdrawn.

35 U.S.C. §103 Rejection

Claims 1 to 3 and 8 to 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,931,408 of Hshieh in view of the disclosure of Ohzone, et al in IEEE, Volume 42, N.1, 1/1995.

The Examiner, however, has misinterpreted the disclosure of Ohzone. Ohzone fails entirely to disclose the use of a two-angle implantation process to form a body region, or indeed any other region in a MOS device. Accordingly, the rejection is unsupported and should be withdrawn.

Before proceeding to discuss the cited references in detail, the Examiner's attention is directed to the fact that the present invention relates to a method for forming a body region in a drain region of a DMOS device on a wafer after a gate has been formed, with the body region extending partly beneath the gate of the DMOS device. An important feature is the fact that implantation of the drain region to form the body region requires two implantation steps, in

which the angle of implantation of one step is different from the angle of implantation of the other step. The two steps as set out in Claim 1 are as follows:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region.

Steps (a) and (b) may be performed in any order, and the dopant of step (a) is to be implanted at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, and the first angle to the surface plane at which the dopant is directed in step (a) is to be less than a second angle to the surface plane at which the dopant is directed in step (b).

In other words, to put a simple label on it, the method of Claim 1 for forming the body region is a two-angle implantation method.

None of the references, by contrast, disclose a method for forming a body region in a DMOS device which requires such a two-angle implantation method. Furthermore, none of the references discloses a two-angle implantation method for forming a body region of any type in any other MOS device, and none of the prior art suggests the possibility of forming a body region in a DMOS or any other MOS device in a two-angle implantation method. Accordingly, regardless of whether the references are considered separately or combined (assuming proper justification for a combination), one would not arrive at the invention of Claim 1.

Applicant does not dispute that Hshieh discloses a method for forming a DMOS transistor which includes forming a conductive gate over a gate oxide, and in turn forming a body region in a drain region after the gate has been formed. Neither does Applicant dispute that Hshieh discloses forming the body region by ion implantation, and then driving in the implanted impurities by a high temperature diffusion process so that the body region extends beneath the gate. *However, as the Examiner accepts, Hshieh fails to teach two implantations for forming the body region by a two-angle implantation method.* The implantation method disclosed by Hshieh for forming the body region is a *single* angle implantation process; and as can be seen from Fig. 8, the implantation is carried out at an angle perpendicular to the surface of the device, or in other words, at a zero degree angle to the vertical.

Turning now in detail to the disclosure of Ohzone, Ohzone entirely fails to disclose the formation of a body region using a two-angle implantation method in any type of MOS device; and certainly, Ohzone fails to disclose the use of a two-angle implantation method for forming a body region in a DMOS device. Firstly, Ohzone is concerned with CMOS devices, namely, CMOSFETs, both n-MOSFETs and p-MOSFETs. Secondly, and most importantly, the disclosure of Ohzone reports on comparative tests which were carried out on two types of CMOSFETs, namely, lightly doped drain (LDD) type n-MOSFETs, and efficient punch through stop (EPS) type p-MOSFETs, where in the case of the n-MOSFETs the LDD region of some of the n-MOSFETs was formed at a 7°-implantation angle, and the LDD region of others of the n-MOSFETs was formed at a 0°-implantation angle, and in the case of the p-MOSFETs the EPS region was formed in some of the p-MOSFETs at a 7°-implantation angle, and the EPS region of others of the p-MOSFETs was formed at a 0°-implantation angle. In other words, Ohzone prepared two batches of n-type MOSFETs, and the LDD region of all the MOSFETs of one batch was implanted at a 7°-implantation angle, while in the other batch the LDD region was implanted at a 0°-implantation angle. Similarly, Ohzone prepared two batches of p-MOSFETs, and in all the MOSFETs of one batch the EPS region was implanted at a 7°-implantation angle, while in the other batch the EPS region was implanted at a 0°-implantation angle. In each batch of both the n-MOSFETs and the p-MOSFETs, MOSFETs of different channel length were fabricated. Having prepared the four batches of MOSFETs, namely, the two batches of n-MOSFETs with the LDD region of one batch implanted at a 7°-implantation angle, and the LDD region of the other batch implanted at the 0°-implantation angle; and the two batches of p-MOSFETs with the EPS region of one batch implanted at the 7°-implantation angle, and with the EPS region of the other batch implanted at the 0°-implantation angle, Ohzone then compared the electrical characteristics of the respective batches of MOSFETs.

Ohzone is thus reminiscent of Contiero, distinguished in a previous response. A single implantation angle is used, though experiments were done at different single angles.

The results of Ohzone's comparison are set out in Figs. 3 to 8. In Fig. 3(a), Ohzone plots the drain current against drain voltage for gate voltages in the range of 1 volt to 5 volts for the n-MOSFETs. The full lines represent the plots of drain current against drain voltage for the n-MOSFETs in which the LDD regions were implanted at the 7°-implantation angle, while the

broken lines represent the plots of drain current against drain voltage for the n-MOSFETs in which the LDD regions were implanted at the 0°-implantation angle. In Fig. 3(b) Ohzone plots the drain current against drain voltage for gate voltages in the range of -1 volt to -5 volts for the p-MOSFETs. The full lines represent the plots of drain current against drain voltage for the p-MOSFETs in which the EPS regions were implanted at the 7°-implantation angle. The broken lines represent the plots of drain current against drain voltage for the p-MOSFETs in which the EPS regions were implanted at the 0°-implantation angle.

In Figs. 4(a) and (b), plots of drain current on a log scale against drain voltage are illustrated for the n-MOSFETs and p-MOSFETs, respectively, of different channel lengths. The full lines of Fig. 4(a) represent the plots of drain current against drain voltage for the n-MOSFETs in which the LDD regions were implanted at the 7°-implantation angle, while the broken lines of Fig. 4(a) represent the plots of drain current against drain voltage for the n-MOSFETs in which the LDD regions were implanted at the 0°-implantation angle. The full lines of Fig. 4(b) represent the plots of drain current against drain voltage for the p-MOSFETs in which the EPS regions were implanted at the 7°-implantation angle, while the broken lines represent plots of drain current against drain voltage for the p-MOSFETs in which the EPS regions were implanted at the 0°-implantation angle. Other electrical characteristics of the n-MOSFETs and p-MOSFETs with their respective LDD regions and EPS regions implanted on the one hand at the 7°-implantation angle and on the other hand at the 0°-implantation angle are illustrated in Figs. 5 to 8.

Manifestly, Ohzone is only concerned with comparing the electrical characteristics of the respective n-MOSFETs and p-MOSFETs where the LDD and EPS regions, respectively, are implanted on the one hand at a single implantation angle of 7°, and on the other hand at a single implantation angle of 0°. *There is absolutely no disclosure in Ohzone of either the LDD regions or the EPS regions being implanted by a two-angle implantation method whereby one of the implantation angles is at 7° and the other is at 0°, or indeed at any other combination of angles.* Ohzone is solely concerned with implanting the LDD regions and the EPS regions at one *single* angle only, which in one case is 7° and in the other case 0°. (See the prior Contiero discussion.)

Furthermore, there is absolutely no suggestion in the disclosure of Ohzone of the possibility of the same LDD region or the same EPS region being formed by implantation at two

different implantation angles. Neither is there even the slightest hint in Ohzone that one could form one of the LDD regions or one of the EPS regions in a two-angle implantation method.

Furthermore, Applicant emphasizes that the analysis and comparisons carried out by Ohzone are on CMOSFETs only. Ohzone is entirely unconcerned with DMOS devices. DMOS devices, as discussed with reference to the disclosure of Han in the response which was filed on April 21, 2003, are entirely different devices, and their functioning is also quite different from that of CMOS devices. However, even if one were to allow that CMOS and DMOS were similar type devices, which Applicant does not accept, the disclosure of Ohzone, as discussed in detail above, fails to disclose the formation of any type of body region in a CMOS device which is formed by a two-angle implantation process.

Therefore, even by combining the two disclosures of Hshieh and Ohzone, one would not arrive at the invention of Claim 1.

Additionally, and not incidentally, no proper basis has been shown to believe one skilled in the art would have been motivated to make such a combination.

Further, as discussed in the response filed on April 21, 2003, secondary considerations point strongly towards unobviousness. The claimed invention has produced a major step forward in the art, notwithstanding its apparent simplicity, since it permits the formation of DMOS devices using conventional CMOS processes, and permits the formation of DMOS devices simultaneously with other CMOS devices. Moreover, the method according to the invention, including steps or acts (a) and (b) of Claim 1, permits the drain/source threshold voltage of a DMOS device to be determined independently of the punch-through breakdown voltage of the device and, indeed, independently of the avalanche breakdown voltage. Consequently, the method of the claimed invention significantly reduces the time and cost of production of integrated circuit chips which include combinations of CMOS and DMOS devices. This advantage is discussed in the specification at page 8, lines 2-12; other corresponding problems of prior art methods are discussed in the specification at page 1, line 10 to page 3, line 10.

Again it is emphasized that despite the existence of the prior art for over four years, which in the semiconductor industry is a significant time period, no one else made the claimed

invention. This substantial time period, coupled with the great advantages of the invention, is powerful evidence of unobviousness and is in no way diluted by the simplicity of the invention.

For the foregoing reasons, reconsideration and withdrawal of the rejection is now requested.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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